## REMARKS

Claims remaining in the present patent application are Claims 1-26. Claims 1, 4, 12 and 22 are amended herein. Applicants respectfully note that no new matter is added as a result of the amendments presented herein. Applicants respectfully request reconsideration of the above captioned patent application in light of the amendments and remarks presented herein.

## Rejection Informalities

The rejection of Claim 17 under 35 U.S.C. § 103(a) depends, in part, upon Belhaj (US 6,564,179, "Belhaj"). Applicants respectfully note that Belhaj is not cited in the "Notice of References Cited" (PTO-892) or in the Form 1449 Information Disclosure provided by Applicants.

In the interest of timely prosecution, this rejection will be addressed subsequently herein. However, Applicants herewith submit Belhaj via an Information Disclosure Statement so that the Examiner may easily document his review of this reference.

## Allowable Material

The Official Action indicates that Claim 26 is allowed. Applicants thank the Examiner for indicating allowed material.

Claims 18-25 are indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants thank the Examiner for indicating allowable material.

## Claim Objections

Claim 1 is objected to because of the informality of an improper article. Applicants respectfully assert that amended Claim 1 corrects this informality, and respectfully solicits allowance of this Claim.

## 35 U.S.C. § 103

The rejections of Claims 1-16 depend, in part, on Circello et al. (US 5,964,893, "Circello"). Applicants respectfully assert that Circello actually teaches away from embodiments of the present invention as recited in Claims 1-16 in view of the following rationale. Claims 1-16 recite, in part, the limitation of "an emulator device." In contrast, Circello teaches:

> Unlike prior art devices which require either an external software monitor program or an external emulator..., the present invention provides data which indicates a current operation of the data processor to an external user (Column 3, lines 45-49, emphasis added).

Thus, Applicants respectfully assert that one of ordinary skill in the art would be taught away from embodiments of the present invention as recited in Claims 1-16 that recite emulation by Circello's teachings against emulation.

For this reason, Applicants respectfully assert that Claim 1-16 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Claims 1-5, 7-8, 10-12, 13 and 16 stand rejected under 35 USC § 103(a) as allegedly unpatentable over Circello et al. (US 5,964,893, "Circello") in view of Bakker (US 6,185,522, "Bakker"). Applicants have carefully reviewed the cited references and respectfully assert that embodiments of the present invention as recited in Claims 1-5, 7-8, 10-12, 13 and 16 are not rendered obvious by Circello in view of Bakker.

With respect to Claim 1, Applicants respectfully assert that Circello does not teach or suggest the limitation "the emulator device implementing the DUT and executing instruction in lock-step with the DUT" as recited by Claim 1. In contrast Circello teaches "an external development system... dynamically observe(s) internal operations of a data processor..." and further, the "external development system... trace(s) an exact program flow..." (Abstract, emphasis added).

Applicants respectfully assert that the rejection improperly equates Circello's system that traces, e.g., records, execution of a device under test with

the recited emulation device that "execute(s) instruction in lock-step with the DUT" as recited by Claim 1. Applicants respectfully assert that Circello does not teach or suggest emulation, as the term is understood in the art. Applicants respectfully assert that one of ordinary skill in the art would understand a fundamental difference between Circello and embodiments of the present invention as recited in the present Claims. Furthermore, Bakker does not correct the deficiencies of Circello.

For this additional reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 2-4 depend from Independent Claim 1. Applicants respectfully assert that these Claims overcome the rejections of record as they depend from an allowable base claim, and respectfully solicit allowance of these Claims.

With respect to Claim 5, Applicants respectfully assert that this Claim overcomes the rejections of record for the rationale previously presented with respect to Claim 1, and respectfully solicit allowance of this Claim.

Claims 6-16 depend from Independent Claim 5. Applicants respectfully assert that these Claims overcome the rejections of record as they depend from an allowable base claim, and respectfully solicit allowance of these Claims.

Claims 9 and 13 stand rejected under 35 USC § 103(a) as allegedly unpatentable over Circello et al. (US 5,964,893, "Circello") in view of Bakker (US 6,185,522, "Bakker") and further in view of Buckmaster et al. (US 6,298,320) and further still in view of Official Notice. Applicants have carefully reviewed the cited references and respectfully assert that embodiments of the present invention as recited in Claims 9 and 13 are not rendered obvious by Circello in view of Bakker and further in view of Buckmaster and further still in view of Official Notice.

Claims 9 and 13 depend from Independent Claim 5. Applicants respectfully assert that these Claims overcome the rejections of record as they depend from an allowable base claim, and respectfully solicit allowance of these Claims.

Further with respect to Claim 9, Applicants respectfully assert that Buckmaster actually teaches away from embodiments of the present invention as recited in Claim 9. Buckmaster teaches "[t]he communications interface 34 includes a conventional Ethernet driver 66 and an Ethernet connector..." (column 6, lines 25-29). Applicants respectfully assert that one of ordinary skill in the art would understand that the signal line limitations set forth in Claim 5, from which Claim 9 depends, are incompatible with conventional Ethernet signal specifications.

For this yet additional reason, Applicants respectfully assert that Claim 9 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claim 6 stands rejected under 35 USC § 103(a) as allegedly unpatentable over Circello et al. (US 5,964,893, "Circello") in view of Bakker (US 6,185,522, "Bakker") and further in view of Coehlo et al. (US 6,223,272). Applicants have carefully reviewed the cited references and respectfully assert that embodiments of the present invention as recited in Claim 6 are not rendered obvious by Circello in view of Bakker and further in view of Coehlo.

Claim 6 depends from Independent Claim 5. Applicants respectfully assert that this Claims overcomes the rejections of record as it depends from an allowable base claim, and respectfully solicit allowance of this Claim.

Claim 14 stands rejected under 35 USC § 103(a) as allegedly unpatentable over Circello et al. (US 5,964,893, "Circello") in view of Bakker (US 6,185,522, "Bakker") and further in view of Young et al. (US 6,107,826). Applicants have carefully reviewed the cited references and respectfully assert that embodiments of the present invention as recited in Claim 14 are not rendered obvious by Circello in view of Bakker and further in view of Coehlo.

Claim 14 depends from Independent Claim 5. Applicants respectfully assert that this Claims overcomes the rejections of record as it depends from an allowable base claim, and respectfully solicit allowance of this Claim.

Further with regard to Claim 14, the rejection argues that one of ordinary skill in the emulation art would be motivated to use "the DLL methods disclosed in the Circello [sic] reference in combination with the emulation methods of the Bakker reference because of the flexible and efficient manner in which clock signals can be routed through out an FPGA." Applicants respectfully assert that embodiments of the present invention are not directed toward routing clock signals throughout an FPGA. Therefore this alleged motivation has no bearing on embodiments of the present invention. Applicants respectfully assert that the taught art for "routing clock signals throughout an FPGA" would not commend itself to one of ordinary skill in the art in considering Applicants' problem.

For this additional reason, Applicants respectfully assert that Claim 14 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claim 17 stands rejected under 35 USC § 103(a) as allegedly unpatentable over Swoboda et al. (US 5,805,792, "Swoboda") in view of Belhaj (US 6,564,179, "Belhaj") and further in view of "ICEBERG: An Embedded In-circuit Emulator Synthesizer for Microcontrollers" by Huang and Lu ("Huang"). Applicants respectfully note that Belhaj is relied upon but not officially cited. Applicants

have carefully reviewed the cited references and respectfully assert that embodiments of the present invention as recited in Claim 14 are not rendered obvious by Swoboda in view of Belhaj and further in view of Huang.

The rejection alleges that the four signal lines SCIN, SCOUT, EC0 and EC1 comprising port 2111 as shown in Swoboda Figure 81 teach a "four-wire interface" as recited and further limited by Claim 17. Applicants respectfully traverse. The rejection is unclear as to which signal line of Swoboda allegedly teaches which of the recited limitations of Claim 17's "four-wire interface."

Swoboda teaches:

> [F]our wire scan interface or port 2111 is connected... to serial data in SCIN 2115 and serial data out SCOUT- 2117 pins. Emulation control pins EC0 and EC1 provide further control inputs. Test modes are controlled via the EC1, EC0 and SCIN pins, and two bits TEST and COMPRESS of the emulation control register 2121. ... The control pins EC1, EC0 and SCIN initially define the state of the emulation control port (column 50, lines 24-51).

Applicants respectfully assert that the described serial data in SCIN line does not teach or suggest the limitation of "a first interface line carrying a system clock driven by the microcontroller, for driving the communication state machines forming a part of the virtual microcontroller" or the limitation of "a

second interface line carrying an internal microcontroller CPU clock" or the limitation of "a third interface line for use by the microcontroller to send I/O data to the ICE and to notify the ICE of pending interrupts" or the limitation of "a fourth interface line for bi-directional communication that is used by the microcontroller to send I/O data to the ICE, and that is used by the ICE to convey halt requests to the microcontroller" as recited by Claim 17.

Applicants respectfully assert that the described serial data out SCOUT line does not teach or suggest the limitation of "a first interface line carrying a system clock driven by the microcontroller, for driving the communication state machines forming a part of the virtual microcontroller" or the limitation of "a second interface line carrying an internal microcontroller CPU clock" or the limitation of "a third interface line for use by the microcontroller to send I/O data to the ICE and to notify the ICE of pending interrupts" or the limitation of "a fourth interface line for bi-directional communication that is used by the microcontroller to send I/O data to the ICE, and that is used by the ICE to convey halt requests to the microcontroller" as recited by Claim 17.

Applicants respectfully assert that the described emulation control pin EC0 line does not teach or suggest the limitation of "a first interface line carrying a system clock driven by the microcontroller, for driving the communication state machines forming a part of the virtual microcontroller" or the limitation of "a second interface line carrying an internal microcontroller CPU clock" or the limitation of "a third interface line for use by the microcontroller to send I/O data

to the ICE and to notify the ICE of pending interrupts" or the limitation of "a fourth interface line for bi-directional communication that is used by the microcontroller to send I/O data to the ICE, and that is used by the ICE to convey halt requests to the microcontroller" as recited by Claim 17.

Applicants respectfully assert that the described emulation control pin EC1 line does not teach or suggest the limitation of "a first interface line carrying a system clock driven by the microcontroller, for driving the communication state machines forming a part of the virtual microcontroller" or the limitation of "a second interface line carrying an internal microcontroller CPU clock" or the limitation of "a third interface line for use by the microcontroller to send I/O data to the ICE and to notify the ICE of pending interrupts" or the limitation of "a fourth interface line for bi-directional communication that is used by the microcontroller to send I/O data to the ICE, and that is used by the ICE to convey halt requests to the microcontroller" as recited by Claim 17.

Neither Belhaj nor Huang correct these deficiencies of Swoboda. For these reasons, Applicants respectfully assert that Claim 17 overcome the rejections of record, and respectfully solicit allowance of this Claim.

Further with respect to Claim 17, Applicants respectfully assert that Belhaj actually teaches away from embodiments of the present invention as recited in Claim 17. Belhaj teaches software emulation of a first processor on a second processor. Consequently, as taught by Belhaj, one microprocessor is both

microcontroller and emulator device. In contrast, Claim 17 recites, in part, "a four-wire interface... to couple a microcontroller with an emulator device." Applicants respectfully assert that one or ordinary skill in the art would be taught away from embodiments of in accordance with the present invention as recited in Claim 17 that recite, in part, coupling "a microcontroller with an emulator device," by Belhaj's teachings that a microcontroller and an emulator device are one in the same.

For this additional reason, Applicants respectfully assert that Claim 17 overcome the rejections of record, and respectfully solicit allowance of this Claim.

## CONCLUSION

Claims remaining in the present patent application are Claims 1-26. Claims 1, 4, 12 and 22 are amended herein. Applicants respectfully note that no new matter is added as a result of the amendments presented herein. The Applicants respectfully request consideration of the above captioned patent application in light of the amendments and remarks presented herein.

Applicant has reviewed the following references that were cited but not relied upon, and does not find these references to show or suggest embodiments of the present invention: US 6,223,144, US 5,493,723, US 5,999,725, US 6,161,199, US 6,263,484, US 6,289,300, US 6,366,878, US 5,889,988, US 6,516,428, US 6,487,700, US 5,559,996, US 6,032,268, DE 19742577 (as understood by Applicants), "Fast Development of Source-level Debugging System Using Hardware Emulation," IEEE 2000 pp 401-404, "FPGA Architectures for ASIC Hardware Emulators," IEEE 1993, pp 336-340, "Emulator environment based on an FPGA prototyping board," IEEE 21-23 June 2000, pp 72-77, "An FPGA-Based Hardware Emulator for Fast Fault Emulation," IEEE 1997 pp 345-348, "An In-Circuit Emulator for TMS320C25,", IEEE 1994, pp 51-56, "In-Circuit-Emulation in ASIC Architecture Core Designs," IEEE 1989, pp P6-4.1-P6.4.4, "Using Background Modes for Testing, Debugging and Emulation of Microcontrollers," IEEE 1997, pages 90-97.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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